

Thermal stability of defect complexes due to high dose MeV implantation in silicon

P.K. Giri ^{a,*}, Y.N. Mohapatra ^b

^a *Dipartimento di Fisica, Università di Catania, 57 Corso Italia, I95129 Catania, Italy*

^b *Department of Physics, Indian Institute of Technology, Kanpur 208016, India*

Abstract

The nature of electrically active defects created by high dose MeV Ar⁺ implantation in epitaxial silicon and thermal stability of these defects have been investigated using capacitance–voltage (C–V) and deep level transient spectroscopy (DLTS) measurements. Unusual C–V characteristics in as-implanted Schottky devices is interpreted taking into account migration and clustering of ion beam generated defects. Using DLTS, a compensating midgap trap of large concentration has been detected in as-implanted deep buried layers of both n-type and p-type silicon. Due to low temperature (160°C) oven annealing of implanted n-Si, the dominant defect related peak in DLTS shifts towards higher temperature indicating deepening of emission energy and increased concentration of electrically active species with annealing time. Furnace annealing of damaged silicon at 400 and 600°C reveals gradual annealing of defects with changes in defect spectra. In n-type silicon the majority of the electrically active defects were annealed after 30 min annealing at 600°C, while a stable defect with high concentration was found in p-type silicon upon annealing. The results indicate that due to annealing, stable defects clusters were formed which introduce energy level in the lower half of the band-gap of silicon and the presence of both majority carrier and minority carrier traps are detected due to possible inversion in the damaged layer. The observed major defects in both n-type and p-type silicon are of common origin, which we attribute to interstitial cluster related, and their size changes with low temperature annealing. © 2000 Published by Elsevier Science S.A. All rights reserved.

Keywords: High dose implantation; Defects; Interstitial cluster; Annealing; DLTS

1. Introduction

A recent thrust in studies of defects induced by high dose irradiation of MeV heavy ions in semiconductors is prompted by its increasing importance in ion beam processing technologies as well as in understanding of several fundamental phenomena specific to high dose irradiation [1]. It is known that in high dose implantation, defects produced in as-implanted layers control subsequent evolution of defects and extent of relaxation of the disordered layers [2]. With the stringent requirements for miniaturization of newest generation devices, to achieve a reduced thermal budget for electrical activation and damage annealing, it is essential to understand the kinetics of formation and thermal stability of ion implantation induced defects.

In case of low dose and/or light ion implantation, simple defects structure involving vacancy, interstitial and impurity complexes are formed and they are usually annealed by ~400°C. However, heavy ion implantation at high fluences causes formation of complex defect structure even at room temperature and can evolve to stable structures at elevated temperature [3]. During heat treatment, simple point defects, which escape direct recombination can agglomerate into clusters and eventually form extended defects [4]. While structural tools such as transmission electron microscopy have been used extensively for such studies, tools sensitive to point defects, which introduce energy level in the band-gap of semiconductors are much less utilized, primarily due to interpretational difficulties. Simulational studies show that interstitials (I) and vacancies (V) generated during high dose implantation tend to interact forming defect clusters either during the implantation process or in the first stage of annealing. Recent electrical studies on self-ion implanted Si using

* Corresponding author. Tel.: +39-95-591-912; fax: +39-95-383-023.

E-mail address: pravat.giri@ct.infn.it (P.K. Giri)

deep level transient spectroscopy (DLTS) analysis on defect evolution [5] and thermal stability of defects [6] have shown electrical signature of interstitial clusters in silicon. However, it was noted that variation in the processing condition resulted in change in defect spectra for these defects in silicon. Therefore, details of the factors governing the kinetics of such processes during defect evolution remains unclear. More recently, there has been attempt to study energetics of self-interstitial clustering in silicon [7]. A correlation of electrical signature of these defects from theory [8] and experiment is lacking in the literature.

In this article, we have investigated the electrical signature of defects in high dose as-implanted n-type and p-type silicon and the thermal stability of these defects after post-implantation annealing. Steady state and transient capacitance measurements have been utilized on Schottky devices with damaged layers embedded in the depletion layer. Unusual features in capacitance–voltage (C – V) and DLTS spectra has been correlated with a high density of electrically active defects in the damaged layer. From DLTS analysis of annealed samples, it is shown that defect spectra evolve during annealing at various temperature in the range 160–600°C and a stable defect with high concentrations form in case of p-type silicon. The origin of these defects are discussed in the light of recent reports from experiments and simulation studies.

2. Experimental

Samples used for this study were epitaxial layers of (i) phosphorous doped n-Si ($\rho \approx 2$ – $5 \Omega \text{ cm}$) and (ii) boron doped p-Si ($\rho \approx 1$ – $3 \Omega \text{ cm}$), grown on heavily

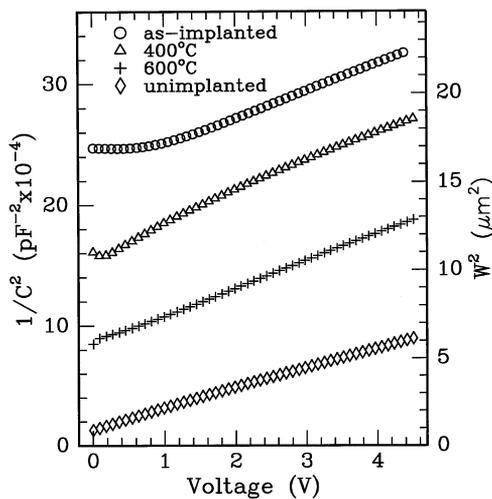


Fig. 1. Comparison of C – V characteristics at room temperature of unimplanted, as-implanted and various annealed (400 and 600°C) n-Si implanted with $5 \times 10^{13} \text{ cm}^{-2} \text{ Ar}^+$ ions. Right-side axis shows the corresponding depletion width (W).

doped layers of Si. The wafers were irradiated from the front side at room temperature using a 2 MeV Van de Graaff accelerator with Ar^+ ions at doses 5×10^{13} and $1 \times 10^{14} \text{ cm}^{-2}$ and an energy 1.45 MeV. Schottky contacts were made by evaporating gold dots of 1 mm diameter. The as-implanted devices did not receive any other high temperature annealing except for heating at 70°C for 30 min for curing the epoxy contact. A few finished devices having implant induced damage were oven annealed at 160°C for 30–180 min to study possible defect evolution/relaxation. To monitor the effect of annealing, two groups of irradiated wafers were annealed in vacuum for 30 min at 400 and 600°C prior to Schottky contact formation. Capacitance measurements were performed using a Boonton capacitance meter operated at 1 MHz and transient data were analyzed using conventional DLTS technique.

3. Results and discussion

3.1. Defects in n-type silicon

Fig. 1 shows a typical $1/C^2$ versus V plot at room temperature for Ar^+ ion irradiated n-Si before and after high temperature annealing. For the unimplanted sample, the curve is linear as expected due to the uniform doping and the zero-bias depletion width is in agreement with the calculated value for the known doping concentration. However, for the as-implanted sample, the zero-bias depletion width is very high compared with unimplanted case and a part of C – V curve is flat, i.e. does not change with voltage. The extent of the flat region and the high depletion width are found to increase with implantation dose. In a previous report [9], it has been shown that these features in the as-implanted device are due to the presence of high density of compensating traps which are located even far beyond the projected ion range. Thus the defect responsible is migrating species related. It is clearly seen from Fig. 1 that high temperature annealing decreases the trap concentration leading to a systematic change in both major features in C – V characteristics. With an increase in annealing temperature, (i) the zero-bias depletion width recovers towards control samples, and (ii) the extent of flat region for low bias reduces progressively. The temperature range of annealing (400–600°C) itself suggest that the dominant defects controlling electrical behaviour are point defects, since extended defects begin annealing at much higher temperature ($> 1000^\circ\text{C}$). The comparison with unimplanted devices shows that 600°C is not sufficient for complete removal of defects.

A typical set of DLTS spectra for as-implanted and low temperature annealed samples are shown in Fig. 2. For the as-implanted sample, two majority carrier trap

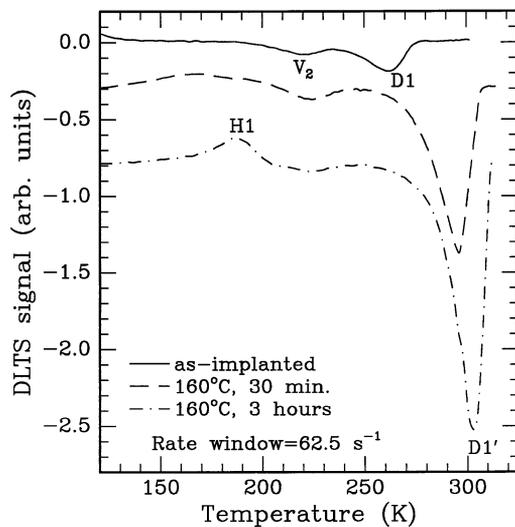


Fig. 2. A set of DLTS spectra for as-implanted and 160°C annealed Ar⁺ implanted n-Si. Minority carrier trap peak is labeled as H1.

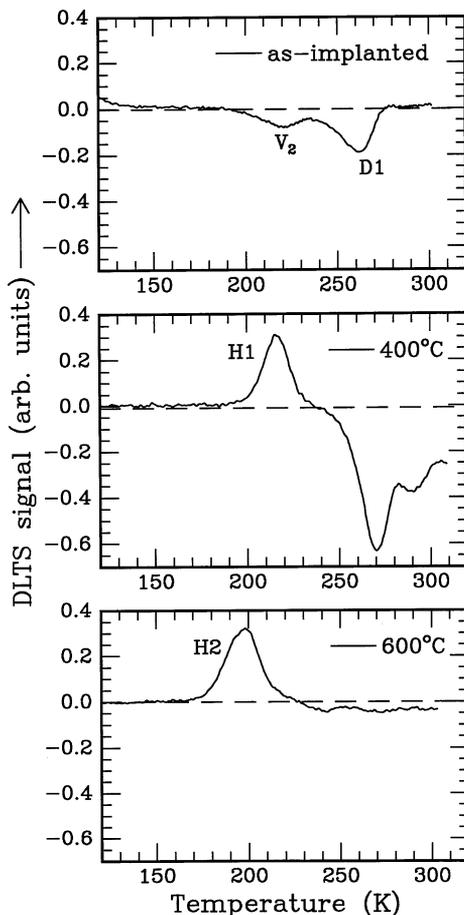


Fig. 3. Comparison of DLTS spectra on as-implanted, 400 and 600°C annealed n-Si for $e_n = 63 \text{ s}^{-1}$. Dashed line shows the base line for distinguishing majority and minority carrier trap peaks.

related peaks labeled V_2 and D1 are observed in the spectra irrespective of ion dose. The peak labeled V_2 is

due to second ionization of the well known divacancy center at energy $E_c - 0.42 \text{ eV}$ with capture cross-section (σ) of $3 \times 10^{-15} \text{ cm}^2$ [10]. The peak labeled D1 is a newly observed trap in as-implanted n-Si which occurs with large concentration. A comparison of the spectra for as-implanted and annealed samples shows several interesting features. With annealing, though V_2 related peak height seems to have reduced without any change of peak position, the D1 peak is shifted towards higher temperature with an increase in peak height. It can be noted that D1' peak shape is substantially narrower and skewed at the right side compared to the as-implanted D1 peak. The shift in peak position in the DLTS spectra implies that low temperature annealing of the damaged layer results in deepening of emission energy or increase in capture cross-section of the dominant defect D1. Such low temperature heat treatment may cause relaxation of the disorder medium surrounding the defects or a change in the defect configuration and correspondingly a change in the energy of the defect. Isothermal transient measurements made in constant capacitance mode, which avoid problems related to high trap density, were analyzed for trap parameter evaluation. Transient measurements made at lower temperature shows a broadening of spectral lineshape. High temperature narrowness of the spectra is ascribed to change in quasi-Fermi level during trap emission [11] which is minimized at low temperature due to a smaller change in trap occupancy. The broadening of the lineshape indicates a distribution in emission energy of the defect D1. From lineshape fitting, a Gaussian broadening of 25 meV for D1 peak is estimated for high dose implanted sample, whereas it is 6 meV for low dose implanted sample. This broadening in energy can be attributed to lattice strain around the defect and in case of defect agglomeration with a size distribution, the energy broadening is naturally expected. It is worth mentioning here that for high dose implanted sample, higher broadening of D1 peak ($\sim 25 \text{ meV}$) compared to broadening of V_2 peak ($\sim 10 \text{ meV}$) [12] is a strong indicator of defect agglomeration being partly responsible for this energy broadening of the D1 level. The fact that the broadening occurs in high dose irradiated samples and does so prior to high temperature annealing, suggest that it is due to intrinsic defect clusters in silicon. Depending on the dose and the annealing (low temperature) conditions, the Arrhenius plot for D1 peak yields an activation energy (E_T) in the range 0.49–0.56 eV measured from conduction band and $\sigma \approx 1 \times 10^{-15} \text{ cm}^2$ [11]. The sensitivity of E_T to annealing conditions and ion dose indicates the marked influence of changes in the environment of the defect and relaxation of the defect structure. In spite of moderate broadening, the peak D1 has a point-defect-like lineshape and corresponds to a well-defined defect.

The effect of vacuum annealing on the irradiated Si at higher temperature is shown in Fig. 3. In contrast to the spectra of as-implanted sample, 400°C annealed sample shows a different DLTS spectrum consisting of two majority carrier trap peaks and one minority carrier trap related peak (H1). The peak position of the major defect is shifted towards the higher temperature side. An estimation of trap activation energy using an Arrhenius plot refers to a midgap trap level with a relatively higher capture cross-section than that of D1 of as-implanted sample. Hence, the major defects created in as-implanted samples are not annealed out by 400°C annealing. By 600°C annealing, these defects are almost annealed out as shown in Fig. 3. However, the presence of a minority carrier trap related peak (H2) can be noted. Though the spectra corresponding to the as-implanted and the 400°C annealed sample showed an apparent increase in peak height of the major trap along with the growth of a minority carrier related peak (H1), C–V measurements on these samples indicated gradual decrease of the defect density with annealing at 400 and 600°C. It can be noted that DLTS spectra shows a small peak height of H2 in the 600°C annealed sample, while C–V characteristic showed substantial

difference between unimplanted and annealed samples. This indicates that not all the defects beyond the effective electrical interface are completely annealed out by 600°C annealing for 30 min. The minority carrier trap filling in this case may be due to a mild inversion caused by compensating trap in the damage layer.

3.2. Defects in p-type silicon

In case of p-type Si samples, defect annealing was monitored mainly through DLTS analysis. Fig. 4 shows a set of DLTS spectra for as-implanted and samples annealed at various temperatures (160, 400 and 600°C) for 30 min. Clearly, all the spectra are different from each other for same rate window. This indicates the formation of new defects/complexes even for low temperature annealing. The defect present after 600°C annealing occurs in a very large concentration as shown in Fig. 4(d). This has been found also in thermally stimulated capacitance measurement which showed large capacitance step at low temperature due to trap emptying. In the as-implanted sample, three majority carrier trap related peaks (P1, P2, P3) and one minority carrier related trap peak (P4) are observed in the temperature range 100–310 K. The conventional Arrhenius plot for peak P1 gives an $E_T = E_v + 0.37$ eV and $\sigma \approx 4 \times 10^{-15}$ cm². This peak corresponds to a hole trap commonly attributed to C_iO_i complex [13]. The peak P2 was found to be broader than that expected from the exponential transient from a discrete level. The trap activation energy obtained from DLTS spectra is $E_v + 0.6$ eV. However, more reliable data were obtained from constant capacitance isothermal spectroscopic measurement which yield $E_T = E_v + 0.52$ eV and $\sigma \approx 9.9 \times 10^{-14}$ cm² [14]. This capture cross-section is rather high for a simple point defect and it may be due to coulomb assisted trapping at the defect site. It is likely that the defect involved may be a multiple trapping site which would be expected from cluster type defects.

Upon low temperature oven annealing the defect spectra is changed as shown in Fig. 4(b). The minority carrier related peak (P4) is not observed after 160°C annealing, while the major peak P2 is shifted to a lower temperature labeled as P2'. Annealing at 400°C results in complex spectra with multiple peaks of relatively smaller height and one minority carrier trap related peak. The DLTS peak at low temperature (~ 110 K) would refer to a shallower level than those found in as-implanted sample. 600°C annealed sample shows a very high concentration of a majority carrier trap peak and a very small concentration of another trap. From DLTS analysis, this major trap was found at $E_v + 0.51$ eV with $\sigma \approx 10^{-12}$ cm². This high value of σ may again refer to coulomb assisted trapping at defect clusters. Note that this value of σ is higher than the σ value

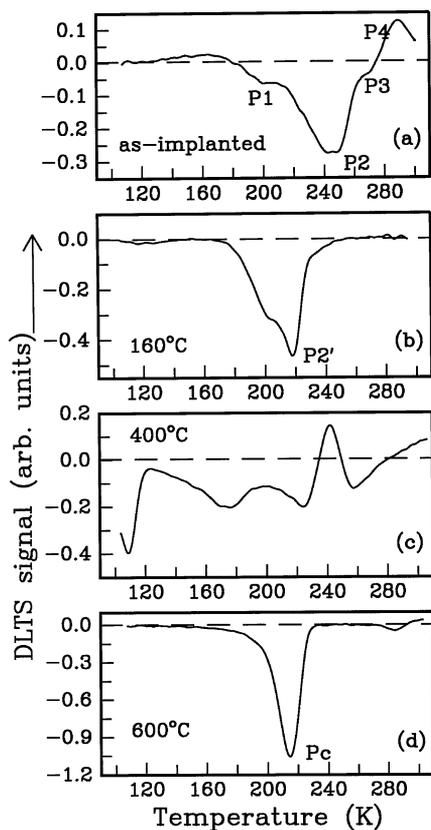


Fig. 4. Comparison of DLTS spectra for (a) as-implanted, (b) 160°C, 30 min, (c) 400°C, 30 min, (d) 600°C, 30 min annealed, Ar⁺ irradiated p-Si. Rate window $e_p = 500$ s⁻¹. Dashed line shows the base line for distinguishing majority and minority carrier trap peaks.

found for the defect in the as-implanted case, which may be due to increased cluster size. The peak related to this level was found to occur at a lower temperature than a similar level reported by Benton et al., who studied defect evolution from point defect to extended defect with high dose self-ion implantation and subsequent annealing [5]. In a more recent study, it was shown that for high dose ($> 10^{13} \text{ cm}^{-2} \text{ Si}^+$) implantation, the defect evolution with annealing is more complex than in the case of lower dose implantation [6]. Therefore, complex evolution of defect spectra, as observed in the present work involving high dose, is in agreement with literature reports. It is interesting to note that the DLTS peak in 600°C annealed p-Si occurs roughly at the same temperature as the H2 peak in n-Si (Fig. 3) for same rate window. Hence, the defect level formed after 600°C annealing lies in the lower half of the band-gap in both n-Si and p-Si.

3.3. Origin of the defects

It is known that interstitial defects migrate much beyond the ion range while vacancy type defects are present in the region modified directly by the ions or the region preceding the implanted ion profile [15]. Vacancies near the surface may easily migrate towards the surface and thus annihilate. As high dose implantation produces a dense collision cascade of displacements, the resulting vacancies and interstitials, which escape direct recombination, may aggregate to form clusters. In the present case, that these defects are detected much beyond the ion range strongly indicate that interstitial clusters are responsible for the observed defect spectra. Because Ar^+ damage is a source of interstitials [16], the involvement of small interstitial clusters such as di-interstitials are strongly indicated in as-implanted case. Studies on cluster formation using molecular dynamics calculations predict the formation of clusters of various sizes which in principle should give rise to a broadening of the electrical activation energies. Our results show a relatively small but detectable broadening, of the energy levels particularly for the high dose case, which could be due to the narrow distribution in cluster sizes and/or inhomogeneous environment in the vicinity of the defect. In the case of p-Si, the defect spectra go through complex changes with annealing and finally yielding a stable defect with large concentration after 600°C annealing. On the other hand, for n-type case the major defect energy deepens progressively with annealing and capture cross-section value also increases. This progressive deepening of energy results in trap levels located below middle of the band-gap and it would be easier to detect such levels in p-type silicon than in n-type silicon through conventional majority carrier

trap filling. It has been predicted from simulation that self-interstitial (I) cluster, particularly four-interstitial (I_4), can introduce energy levels in the lower half of the band-gap of silicon [8]. Our results are in qualitative agreement with such predictions. It is important to mention here that in the DLTS spectra, the major peak D1 of n-type Si (Fig. 2) and the minor peak P4 of p-type Si (Fig. 4) have the similar time constant of emission at fixed temperature, which was analyzed through isothermal spectroscopic analysis. Similarly, in annealed samples, the peak H2 in Fig. 3 and the peak Pc in Fig. 4 have the same time constant at a fixed temperature and it corresponds to a trap level in the lower half of the band-gap. Hence, the major defect in both n-type and p-type as-implanted and 600°C annealed silicon are of the same origin and we attribute it to interstitial cluster related. We do not observe any explicit signature of extended defects either in terms of very broad peak structure in the defect spectra or logarithmic filling of occupancy. The annealing temperature of 600°C may not be sufficient for the formation of extended defects.

4. Conclusions

High dose Ar^+ implantation induced defects and their thermal stability have been studied in both n-type and p-type silicon. In as-implanted silicon, the defect spectrum is dominated by a midgap compensating trap. This trap is speculated to be due to small interstitial cluster such as di-interstitials. Low temperature annealing is shown to change the defect spectrum with progressive deepening in emission energy of the major trap, which points to the relaxation of the defect structure and medium surrounding the defects. A small broadening in activation energy of the major trap is ascribed to the narrow distribution of stable cluster sizes or an inhomogeneous environment in the vicinity of the defect. High temperature vacuum annealing up to 600°C shows complex evolution of the spectrum, particularly in p-type silicon and one stable defect with high concentration is found from DLTS spectra. In contrast, absence of detectable peak in DLTS spectra for annealed n-type silicon indicates that major defects are annealed out by 600°C , 30 min annealing. However, presence of minority carrier trap peak and distinct difference in C–V characteristics of unimplanted and annealed samples indicate that defects levels are introduced in the lower half of the band-gap. Large capture cross-sections of the defects indicate coulomb assisted trapping in cluster type defects in both n-type and p-type Si. These studies reveal significant aspect of variation in defect spectra with evolution of the interstitial cluster size.

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