INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

Department of Computer Science and Engineering

CS523 (Advanced Computer Architecture): End Semester Examination

Date: 18th Sep 2012 Time: 2.00PM-4.00PM Full Marks: 70 Answer all questions

1. [21] **Superscalar Processor**
   a. What is an out of order processor and out of order memory request? What is basic difference between Tomasulo's approach and score board based of instruction scheduling? [3+3]
   b. Calculate available ILP in the following program and what are the limiting factors in compiler and processor to achieve this? [5]

```
for(i=0;i<100;i++){
      A[i]=B[i]+5; //R1= *B; R2=R1+5; *A=R2; A++, B++;
}    //if you unroll the loop, some changes require
```

   c. What are the extra architectural changes required to implement SMT in superscalar processors [3].
   d. Assume 4 issue, aligned window, issue bound opened fetch policy super scalar processor with renaming. Identify registers to rename to remove all false data dependency for the following code. [7]

```
DIV   F0, F2, F4
ADD   F6, F0, F8
ST    F6, O(R1)
SUB   F8, F10, F24
MUL   F5, F10, F8
ST    F5, O(R1)
SUB   F8, F10, F12
MUL   F6, F10, F8
```

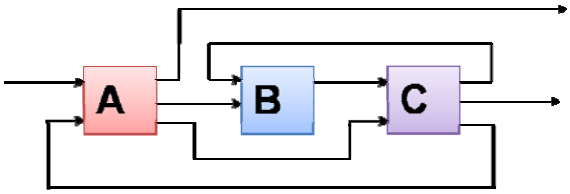
2. [16] **Cache and Memory Hierarchy Design**
   a. Suppose we want to access L1 cache in pipeline manner to improve the performance. Divide the cache access data path of cache in to pipeline stages (may be 3 or 4) and design your improved pipelined L1 cache. [8]
   b. Calculate the average memory access time of cache system with given parameters of memory system. [8]

L1	Miss probability (0.3), Write through, Write probability =0.3, Load forward policy, Read policy is simple and forward. No miss/hit under miss, Read miss address is random in the block, write not allocate, and block size is 100 words. TAccessL2=10ns, Tb=1ns, data width 1 word.
L2	Miss rate is 0.0, Total hit, Miss Penalty is 20ms Write Back
Memory	Write Back, 1000ms

3. [33] **Pipeline Design**

a. Suppose we want to design a pipelined adder (32 bit, 8 stages) with basic ripple carry adders. Suppose a full adder delay is 1ns and clock skew is 10%, setup time is 0.1s. What kind of pipelining is suitable for this and why? [8]

b. Given a non linear pipeline as shown in following figure and given reservation table for instruction X. Find out collision vector and minimum average latency schedule for instruction X. [8]



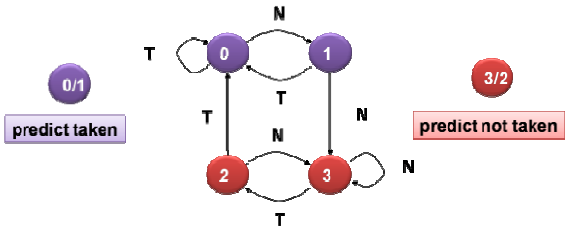
A	X		X		X	
B		X				X
C				X		

c. Calculate the number of branches will be executed for the following C Code. Reduce the number of branches as much as possible for the same and calculate the reduced number of branches.

```
for(i=0;i<10000;i++){
     if(i%2==0) A[i]++;
     else A[i]--;
}
```

Rewriting of code is allowed and if you are using loop unrolling then factor is bounded by 4 (4 time unrolled is allowed). [2+4]

Suppose if you have a two bit branch predictor for each branch, calculate number of miss prediction of original code and your modified/rewritten code. [3+2]



d. Suppose a processing system with a dynamic branch predictor using Branch Target Capture (BTC: BTAC/BTIC). BTC hit is used as prediction means if a hit in BTC then it predict to go for target else predict goes to inline.

A program has 20,000 instructions to run, branch probability is 0.22 (only 2,200 are branch instructions) and it uses BTAC scheme for branch prediction. Used BTAC has hit ratio =0.8, program probability of going to target = 0.7, delay of GIGT=5, delay GIGI=0, delay GTGI=4, delay GTGT=3 then calculate overall branch performance and program performance in term of number of cycles.

What will be performance if BTIC is used instead of BTAC where we save two cycles for going to target case? [5+1]