CS224 : Assignment 2

Date of Demonstration 31st Jan 2023, Lab Timing (2PM-5PM), 14% (7%+ 7%) weight

Part I (Breadboard and IC part)

Implement and Demonstrate a **Four Bit Up-Down Binary Counter** using Breadboard, ICs, and Hookup Wires. ***You are not allowed to use inbuilt counter ICs***. Use FFs, Gates, and other components to design your Counter. Show counter outputs to LEDs of the breadboard. Use the manual clock (using switches) or automatic clock available in the breadboard for demonstration purposes. Using automatic clocks has a higher weight-age.

New additional information: any basic counter working demo will have 70% of marks, 30% of marks are for additional features (up-down counter, synchronous, present, clear, loading, etc) and optimization.

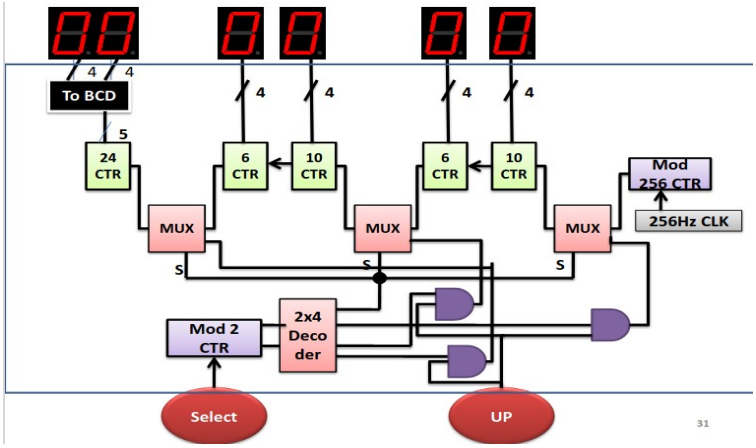
Part II (VHDL and FPGA)

Implement a **Digital Watch** using HDL (either VHDL or Verilog), synthesize and simulate your design entry. After that Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.

Design the **Digital Clock to display time in HH : MM :SS format**, should support Reset/Adjust of time using selectable switch (a) Button 1 for select the Mod Ctr, (b) Button 2 for increasing selected mod Ctr.
Ref: http://jatinga.iitg.ac.in/~asahu/cs221/Lects/Lec04.pdf

Example Design

Design a scaler (scaledown/counter) circuit to generate 1Hz signal from From the FPGA PPL clock (may be MHZ, or 256Hz) and provide that to input to your clock design.



Implement any behavioral model (using +, mod operations) **and/or** structural model (using FFs, Gates and interconnection) **and/or** data flow model for your counters/mux/bcd unit/. Also try to use automiatic (utomatic clock available in the FPGA board (you may need to scale down to 1Hz) or manual clock (using switches). Automatic clock have higher weight-age.
If your FPGA board have only four 7segment display use for MM:SS and use simple LED for hours.

Evaluation Procedure

- All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration (as it is difficult to remember faces of all the 128 students of your batch).
- Grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of chip used,(e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation.
- For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation.

Helps

List of IC available in our LAB: http://jatinga.iitg.ernet.in/~asahu/cs223/ICs-HWLAB-CS223.pdf
We will issue up to two FPGA Boards (Maximum of one BASYS/one ZYBO/one ATLYS/one Nexys A7) for each group for the whole semester.