Assignment 2 : Weightage=20 %Marks, Time= 9 Lab Hours, Demo will be on 17th Feb 2017 and 24th Feb 2017. (Early demonstration is better for your mid-sem exam)

Part (a): Design and implement a 8 bit unsigned multiplier (using ICs and breadbard), and Part (b): Design HDL model and simulate find Operations on n integer numbers and demonstrate using FPGA boards

a. [50% Marks] Design and Implement 8 bit unsigned multiplier (using ICs and breadbard). Display all the outputs in 7 Seg LEDs, except the carry out. Hints: **Algorithm discussed in CS221 (http://jatinga.iitg.ernet.in/~asahu/cs221/Lects/Lec19.pdf) and Assignment is same as last year asssignemnt :) :)** http://jatinga.iitg.ernet.in/~asahu/cs223-2014/
   - Assume both the inputs are unsigned 8 bit integer and produce a 16 bit unsigned integer output
   - Use two 4 bit Adders/ALUs to do addition operations
   - Use DIP switches for inputs (You can issue DIP switches from H. Nath)
   - Use combination of both SIPO and PISO to make full fledged universal shift register (8 bit)
   - For multiplicand (A of AxB), you can use two 4/5 bit PIPO registers
   - For controller you can use a mod 8/16 counter
   - Combination of D-FFs/Latches can be used as register if necessary
   - If you are not getting sufficient number of Seven Segment LEDs then used LEDs of Breadboard for output

b. [50% Marks] **Design HDL model and simulate find OPERATIONS on N integer numbers using Xilinx ISE/Vivado and finally download your design to Digilent ATLYS/BASYS3 FPGA boards and demonstrate.**
   - You are allowed to use FP core generator or LogiCORE IP Floating-Point Unit
   - The operations are SUM, AVERAGE, SUM OF SQUARE, STANDARD Deviation of N Numbers
   - Display the integer part of result in LED or 7Seg LED display of FPGA BOARD
   - Read N (N<10) integers from Switches, initially, Store them in memory.
   - After storing them in memory, calculate the OPERATIONS and store them in at different memory location or in registers
   - Display the results with select options from Switches
     - If select switches is 00 ==> Display SUM
     - If select switches is 01==> Display AVG
     - If select switches is 10==> Display SUMSQ
     - If select switches is 11==> Display SD
   - **Demonstrate your result with both RTL model and behavioral models. Report the maximum frequency at which your design can be used.**