CV of Aryabartta Sahu http://www.iitg.ac.in/asahu/

Educational Qualifications

- Ph. D. Computer Science & Engg. IIT Delhi, 2009
- M. Tech. Computer Science (Utkal University, 2003, 1st class distinction)
- M. Sc. Electronics (Sambalpur University, 2000, 1st class distinction, **Gold Medal, GATE in ECE**)
- B. Sc. Physics, Sambalpur University, 1998, 1st class with distinction
- Matric and Intermediate with 1st class from BSE and CHSE, Orissa

Employments

- IIT Guwahati: Assistant Professor (Dec2009-Apr2016), Associate Professor (Apr2016-till date)

Research Interest

- High Perf. Comp., **HPC for ML,** Cloud/Edge/IoT System, **Multi-Core System**
- **Energy/QoS/Cost Optimization in Cloud/Edge/IoT System** from Task Scheduling Prospects
- **Embeded System**, SoC Components with **Device Driver and OS**, EDA Flow and FPGA System

HPC and Programming Activity

(a) Setup GPU cluster using two GTX 690 GPU, one GTX 980Ti, one AMD Radeon 270x. (b) Setup Intel Xeon Phi for OpenMP, MPI, and Cilk program acceleration, (c) Setup of MPI cluster and local cloud system (d) Developed a new High-Performance Computing (HPC) elective course, (e) Conducted many hands on workshops on MPI and OpenMP programming (f) Executive committee members of IITG Param-Ishan/kamarupa Supercomputer, (g) Conducted workshops on Cuda programming in collaboration with Nvidia Ltd, on Xilinx FPGA in collaboration with Xilinx, on Intel FPGA and Intel Xeon Phi for MPI/TBB prog. in collaboration with Intel India Pvt. Ltd.. (h)Designed and run Computer Peripheal and Interfacing course *which involves **Timer, Peripheral Controller, Interrupt Controller, DMA, UART, BUS, PCI, Video Controller, etc.)***

Research Publication (recent one) and Ongoing works

- **Published 15 Journals papers (12 are in Q1 journal of SCIMAJO).** These papers published in IEEE Trans. on Emerging Topics of Comp. (TETC), Future Gen Comp System (FGCS), Applied Soft Computing (ASC), IEEE System Journal (SysJor), Journal of System Architecture (JSA), Sustainable. Computing (SUSCOM), Computing (COMP), J. Electronic Testing (JETTA), IET Computer. Digit. Tech.

- **Published 11 Conference papers (recent ones).** All these papers published in IEEE/ACM CCGrid, IEEE/ACM DATE, IEEE HPCC, IEEE ANTS and IEEE VLSI Design.

- **Selected Six Publish Papers**
  - Soft Reliability Aware Scheduling of Real-time Applications on Cloud with MTTF constraints, In IEEE/ACM CCGrid 2023
  - Reliability-Ensured Efficient Scheduling With Replication in Cloud, IEEE System journal, 2022
  - Run-time Adaptive Data Page Mapping: A Comparison with 3D-stacked DRAM Cache, J. Syst. Archit, 2020
  - Performance and Area Trade-Off of 3D-Stacked DRAM Based Chip Multiprocessor with Hybrid Interconnect, IEEE Trans. Emerg. Top. Comput. 2021
  - A Comparison of Different Meta-Heuristics for the Quadratic Assignment Problem in Accelerated Systems, Appl. Soft Comput, 2021
  - Efficient Profit Maximization in Reliability Concerned Static Vehicular Cloud System, FGCS 2025
- **On-going works:**
  - Effectiveness and Design of Multiple Row Buffer DRAM System (Submitted to CASES 25)
  - QoS Aware Mixed-Criticality Task Scheduling in Vehicular Edge Cloud System
  - Reliability and Energy Aware Dynamic Scheduling of Workflow in Cloud(submitted to RTCSA)

PhD/MTech/BTech Thesis Supervision

PhD Completed

- Chinmaya Kumar Swain, "Efficient Task Scheduling on Cloud Environment", Defended on 30-07-2021, **currently working at IIM Jammu**.
- Rakesh Pandey, "Efficient Mapping of Multi-threaded Workloads on to Chip Multiprocessors", Defended on 29-07-2020, c**urrently working at Synopsis, Bangalore**
- MS Vasudevan, "Enhancement of SBST Techniques for Detection of Processor Faults", Defended on 29-06-2020, Joint with S. Biswas, **currently working at Infineon Tech, Germany**
- Manojit Ghose, "Energy Aware Online Task Scheduling on Multi-cores Cloud System", Defended on 04-12-2018 joint with S. Karmakar, **currently working at IIIT Guwahati**

PhD Ongoing

- K. Chitra, Efficient Design and Request Scheduling in DRAM System, From Dec-2020
- Suvarthi Sarkar, Efficient Job Scheduling in Vehicular Cloud System, From Aug-2021
- Shubradeep Roy, Data Placement and Job Scheduling in Edge-Cloud System, From Aug-2021
- Vasantha Reddy, Profit and Reliability Aware Request Management in Cloud, From Jan-2022

M. Tech Thesis Supervision: 45 MTP thesis supervised

B. Tech Thesis Supervision: 34 BTP theses.

From last five years, I am able to attract top quality B Tech students (CGPA above 9.0) for their BTPs. I take elective course of B Tech 3rd year where I cover the basic of HPC and seminal papers of the area. And in their BTP, for initial two months of their BTPs, we read 8 to 10 recent top quality papers and find out our own problems to solve and solve in the BTP work.

Sponsored projects: List of Selected Projects

- Design and Development of AI/ML Co-Processor and Post Quantum Cryptography Co-Processor, Meity, **Rs 19.99 Cr**, Apr-2023 to Apr 2026 as Co-PI
- Intel Centre of Excellence on Electronics System Design (Based on Intel FPGA), **Intel India Pvt Ltd**, **Rs 3.5Cr**, Dec 2021-Dec 2025 as Co-PI
- AI Enabled Advanced Aquaponics Ecosystems for the Self-Reliance of SC community in Central and Lower Assam, **DST**, **Rs 2.68Cr**, Apr-21 to Apr-24, as Co-PI
- Design and Development of Image Processing Algorithms on GPUs for X-Ray based Imaging System, **BARC/DAE**, Rs 3.9L, Jul 2015- Jul 2016 as PI
- Task and data mapping on 3D stacked memory large chip multiprocessor (LCMP). IIT Guhahati, 4.8Lakhs, as PI
- Training Program on Cloud System, Imarticus learning Pvt Ltd, 2.95L, May 2023 to May 2024, as PI

Course Taught

- **System Courses** : Operating System (200 students, 2 times), High-Performance Computing (6 times, around 180 students), Advanced Compiler: Auto-paralleling compiler using LLVM (1 time), *Comp. Peripherals & Interface (1 time)* ***which involves Timer, Peripheral Controller, Interrupt Controller, DMA, UART, BUS, PCI, video controller, etc.***
- **Hardware Courses:** Digital Design (200 students, 5 times), also offered as NPTEL course, Hardware Laboratory (6 times), Comp. Org. & Architecture (2 times), Adv. Computer Architecture (1 time),
- **Basic Computing Courses:** Python Programming Lab (1 time), Programming Language Lab (2 times), Introduction to Computing (800 students, 3 times), Computing Laboratory (800 students, 2 times).

For most of the courses lecture slides, Ref book, Exam Question Papers with Solutions and Assignments are available at **http://www.iitg.ac.in/asahu/**

Publications in Journals (recent ones)

1. Suvarthi Sarkar, Akshat Arun, Harshit Surekha, Aryabartta Sahu: Efficient Profit Maximization in Reliability Concerned Static Vehicular Cloud System, Accepted in Future Generation Computer Systems, **FGCS, IF=6.2, SCIMAJO Q1**
2. Rakesh Pandey, Aryabartta Sahu: Performance and Area Trade-Off of 3D-Stacked DRAM Based Chip Multiprocessor with Hybrid Interconnect. *IEEE Transaction on Emerging Topics of Computing*. 9(4): 1945-1959 (2021) **TETC, IF=7.691, Scimajo Q1**
3. Chinmaya Kumar Swain, Ravi Shankar, Aryabartta Sahu: Edge data distribution as a network Steiner tree estimation in edge computing. *Computing 106(5): 1585-1609 (2024)**, Scimajo Q1***
4. Manoj Kumar, Aryabartta Sahu, Pinaki Mitra: A comparison of different metaheuristics for the quadratic assignment problem in accelerated systems. *Applied Soft Computing*. 100: 106927 (2021), **ASC, IF=6.725 , Scimajo Q1**
5. Chinmaya Kumar Swain, Aryabartta Sahu, Reliability Ensured Efficient Scheduling With Replication in Cloud Environment, *IEEE System Journal*, 2021, **SysJour, IF=3.91, Scimajo Q1**
6. Rakesh Pandey, Aryabartta Sahu: Run-time adaptive data page mapping: A Comparison with 3D-stacked DRAM cache. *Journal of System Arch. 1*10: 101798 (2020), **JSA, IF=3.77, Scimajo Q1**
7. Manojit Ghose, Aryabartta Sahu, Sushanta Karmakar: Urgent point aware energy-efficient scheduling of tasks with hard deadline on virtualized cloud system. *Sustain. Computing: Informatics System*, 28: 100416 (2020) **IF=4.028 , Scimajo Q1**
8. Manojit Ghose, Sawinder Kaur, Aryabartta Sahu: Scheduling real time tasks in an energy-efficient way using VMs with discrete compute capacities. *Computing* 102(1): 263-294 (2020), **IF=2.95, Scimajo Q1**
9. Chinmaya Kumar Swain, Aryabartta Sahu: Interference Aware Workload Scheduling for Latency Sensitive Tasks in Cloud Environment. *Computing* 104(4): 925-950 (2022)**. IF=2.95, Scimajo Q1**
10. Chinmaya Kumar Swain, Neha Saini, Aryabartta Sahu: Reliability aware scheduling of bag of real time tasks in cloud environment. *Computing* 102(2): 451-475 (2020) 2**020, IF=2.95, Scimajo Q1**
11. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: RSBST: an Accelerated Automated Software-Based Self-Test Synthesis for Processor Testing. *J. Electron. Test.: Theory and Application* 35(5): 695-714 (2019) **JETTA, IF=1.01**
12. Vasudevan MS, Santosh Biswas, Aryabartta Sahu: Automation of Test Program Synthesis for Processor Post-silicon Validation. J *J. Electron. Test.: Theory and Appl* 34(1): 83-103 (2018) , **JETTA, IF=1.01**
13. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: Fragmented software-based self-test technique for online intermittent fault detection in processors. *IET Comput. Digit. Tech.* 15(1): 56-76 (2021), **IF=0.818**
14. C. K. Swain, Bhawana Gupta, Aryabartta Sahu: Constraint aware profit maximization scheduling of tasks in heterogeneous datacenters. *Computing* 102(10): 2229-2255 (2020)**, IF=2.95 , Scimajo Q1**
15. Tarun K. Agrawal, Aryabartta Sahu, Manojit Ghose, R. Sharma: Scheduling chained multiprocessor tasks onto large multiprocessor system. *Computing* 99(10): 1007-1028 (2017)**, IF=2.95, Scimajo Q1**
16. Manojit Ghose, Aryabartta Sahu, Sushanta Karmakar: Energy Efficient Online Scheduling of Real Time Tasks on Large Multi-threaded Multiprocessor Systems. *J. Inf. Sci. Eng.* 34(6): 1599-1615 (2018), IF=0.541

Publications in Conference

1. K. Chitra, Arjun Dey, Aryabartta Sahu, Minesh Patel: Multiple Row Buufer DRAM, **Accepted in IEEE/ACM Design AutomationConfrence (DAC), Late Bracking Result, 2025**.
2. K. Chitra, Arjun Dey, Aryabartta Sahu: Efficient Mitigation of DRAM Row Buffer Conflict using Request Clustering in Manycore Systems, **IEEE VLSI Design 2025**.

3. Manojit Ghose, Gandhi Preet, Aryabartta Sahu: Maximizing Profit of the Service Providers through Efficient Content Placement and Retrieval in an IoT-enabled Edge-Cloud Platform, **IEEE ANTS 2024, Best Paper Award**.

4. Manojit Ghose, Krishna Prabin Pandey, Niyati Chaudhary, Aryabartta Sahu**:** Soft Reliability Aware Scheduling of Real-time Applications on Cloud with MTTF constraints, **in IEEE/ACM CCGrid 2023.**

5. *Shubhradeep Roy, Suvarthi Sarkar, Aryabartta Sahu:* Profit Maximization Using Collaborative Storage Management in Multi-Tier Edge-Cloud System. *I**EEE HiPC 2023**: 309-318*

6. A Sahu: Temperature Aware Scheduling and Mapping of Multiphase Application on to Chip Multiprocessor, in *ACM/IEEE Design automation and Test in Europe, (DATE 2016)*, **(single author)**

7. Aryabartta Sahu, M. Balakrishnan, Preeti Ranjan Panda: A generic platform for estimation of multi-threaded program performance on heterogeneous multiprocessors. **DATE 2009:** 1018-1023

8. Avadhesh Sharma; Chinmaya Kumar Swain; Aryabartta Sahu: Efficient Welfare Maximization in Fog-Edge Computing Environment; *IEEE HPCC/SmartCity/DSS 2021*, **Core Ranking B**

9. Chinmaya Kumar Swain; Vaibhav Gupta; Aryabartta Sahu : Energy Efficient and QoS Aware Multi-Level Mobile Cloud Offloading, *IEEE HPCC/SmartCity/DSS 2021*, **Core Ranking B**

10. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: Automated Low-Cost SBST Optimization Techniques for Processor Testing. *IEEE VLSI Design 2021*: 299-304

11. Rakesh Pandey, Aryabartta Sahu: Access-Aware Self-Adaptive Data Mapping onto 3D-Stacked Hybrid DRAM-PCM Based Chip-Multiprocessor. *IEEE HPCC2019*: 389-396, **Core Ranking B**

12. Vasudevan M. S, Santosh Biswas, Aryabartta Sahu: RSBST: A Rapid Software-Based Self-Test Methodology for Processor Testing. I*EEE VLSI Design 2019*: 112-117

13. Chinmaya Kumar Swain, Aryabartta Sahu: Interference Aware Scheduling of Real Time Tasks in Cloud Environment. *IEEE HPCC/SmartCity/DSS 2018*: 974-979, **Core Ranking B Catagory**

14. Manojit Ghose, Pratyush Verma, Sushanta Karmakar, Aryabartta Sahu: Energy Efficient Scheduling of Scientific Workflows in Cloud Environment. I*EEE HPCC 2017*: 170-177

15. Sawinder Kaur, Manojit Ghose, Aryabartta Sahu: Energy Efficient Scheduling of Real-Time Tasks in Cloud Environment. *IEEE HPCC/SmartCity/DSS 2017*: 178-185

16. Rakesh Pandey, Aryabartta Sahu: Efficient Mapping of Multi-threaded Applications onto 3D Stacked Chip-Multiprocessor. *IEEE HPCC/SmartCity/DSS 2017*: 324-331

17. Aryabartta Sahu, Saparapu Ramakrishna: Creating heterogeneity at run time by dynamic cache and bandwidth partitioning schemes. SAC 2014: 872-879

Administration Activity at IIT Guwahati

- **Department Level :** Convener PG Admission Committee, DPPC Member, Dept Laboratory In-charge, Invigilation Duty allocation, TA Duty Allocation, Depart Library in Charge, Compute Server setup and procurement committee, and Managing CAES Group Website
- **Institute Level :** Members Library Committee and Members of HPC Executive Committee at IITG

Workshops/Conferences Organized

- Nvidia GPU HPC Workshop Xilinx FPGA Workshop and Computer Architecture Lecture series,
- Intel Xeon Phi High-Performance Workshop, Intel FPGA Faculty Dev. Program (intelfdp)
- Served as Finance Chair and Publication Chair and co-hosted online of **VLSI Design 2021**,
- Program, VDAT (Website Chair) May 2016,
- OPENROAD for Low Cost ASIC Design for Rapid Innovation, Jan 2024
- Eighth International Conference on Information Systems Security (ICISS 2012), IIT Guwahati, India ICISS 2012 (Role as Publicity Chair)